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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,012	11/13/2003	Jen-Yi Hu	10070-US-PA	1011

31561 7590 06/09/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
KOVALICK, VINCENT E	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 06/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,012	HU ET AL.	
	Examiner	Art Unit	
	Vincent E. Kovalick	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-11 and 13-17* is/are rejected.

7)☒ Claim(s) *6 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's Patent Application, Serial No. 10/707,012, with a File Date of November 13, 2003.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 7, 13 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato (Pub. No. US 2002/0140643) taken with Kunori et al. (USP 6,144,584).

Relative to claims 1, 7 and 13, Sato **teaches** a Display Module (pg. 1, paras. 0015-0017); Sato further **teaches** a structure of reducing source line resistance, suitable for use in a light emitting diode display that comprises a plurality of pixels, each of which comprises a light emitting diode, a source and a source line for providing required power to drive the light emitting diode (pg. 5, paras. 0077-0078).

Sato **does not teach** an insulation layer on the source line, the insulation layer having at least two openings exposing two ends of a part of the source line; and at least a conductive layer covering the insulation layer and electrically connected to the source line via the openings, such that the conductive layer and at least the part of the source line are connected in parallel.

Kunori et al. **teaches** a non-volatile semiconductor memory device (col. 5, lines 30-67 and col. 6, lines 1-34); Kunori et al. further **teaches** an insulation layer on the source line, the insulation layer having at least two openings exposing two ends of a part of the source line; and at least a conductive layer covering the insulation layer and electrically connected to the source line via the openings, such that the conductive layer and at least the part of the source line are connected in parallel (col. 42, lines 44-53).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Sato the feature as taught by Kunori et al. in order to put in place the means for reducing source line resistance to provide a stable and uniform driving voltage supplied to each pixel of the LED display.

Regading claim 15, Kunori et al. further **teaches** the feature wherein two neighboring ones of the openings are formed on two ends of a part of the source line (Fig. 51B, items 132).

Relative to claim 16, Sato further **teaches** the step of forming the conductive layer further comprises forming a plurality of conductive segments to fill the openings (Fig. 1, item AD).

It being understood that the conductive layer making contact with the source line SD through the hole is repeated for each of the LEDs.

4. Claims 2, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato taken with Kunori et al. as applied to claims 1, 7 and 13 respectively in item 3 hereinabove, and further in view of Lee (USP 6,133,103).

Regarding claims 2, 8 and 14, Sato taken with Kunori et al. **does not teach** the said structure wherein the conductivity of the conductive layer is large than that of the source line.

Lee et al (USP 6,133,103) **teaches** method for fabricating a mask ROM that improves the level of uniformity of cell voltages (pg 3, lines 46-67 and col. 4, lines 1-12); Lee further **teaches** the said structure wherein the conductivity of the conductive layer is large than that of the source line (col. 4, line 67; col. 5, lines 1-8 and Fig. 7A). It being understood that conductive layer having a low resistivity equates to a higher conductivity level.

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Sato taken wity Kunori et al. the feature as taught by Lee in order to facilitate maintaining a uniform voltage across the source line.

5. Claims 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato taken with Kunori et al. as applied to claims 1, 7 and 13 respectively in item 3 hereinabove, and further in view of Lai (USP 6,875,645).

Relative to claims 3 and 9, Sato taken with Kunori et al. **does not teach** the said structure wherein the conductive layer comprises a plurality of conductive structures distributed between the pixels.

Lai **teaches** pixel structure (col. 2, lines 23-67); Lai further **teaches** the said structure wherein the conductive layer comprises a plurality of conductive structures distributed between the pixels (col. 3, lines 47-67 and col. 4, lines 1-15).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Sato the feature as taught by Lai in order to put in place the means to distribute the proper driving signals to each of the LEDs in the display system.

6. Claims 4, 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato taken with Kunori et al. as applied to claims 1, 7 and 13 respectively in item 3 hereinabove, and further in view of Tomisawa (USP 4,742,254).

Regarding claims 4, 10 and 17, Sato taken with Kunori et al. **does not teach** the said structure wherein the source line comprises a major source line to connect with the source and a plurality of branch lines to supply the power to the light emitting diode of each pixel.

Tomisawa **teaches** an integrated circuit for signal delay (col. 2, lines 13-67 and col. 3, lines 1-13); Tomisawa further **teaches** the said structure wherein the source line comprises a major source line to connect with the source and a plurality of branch lines to supply the power to the light emitting diode of each pixel (col. 4, lines 24-32).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Sato taken with Kunori et al the feature as taught by Tomisawa in order to put in place the power distribution network necessary to supply each of the LEDs.

7. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato taken with Kunori et al. in view of Tomisawa as applied to claims 4 and 7 respectively in item 6 hereinabove, and further in view of Lee.

Relative to claims 5 and 11, Sato taken with Kunori et al. in view of Tomisawa **does not teach** the said structure wherein the conductive layer comprises at least a conductor locate over the major source line.

Lee **teaches a** method for fabricating a mask ROM that improves the level of uniformity of cell voltages (pg 3, lines 46-67 and col. 4, lines 1-12); Lee further **teaches** the said structure wherein

the conductive layer comprises at least a conductor locate over the major source line (col. 4, lines 44-67, col. 5, lines1-8 and Fig. 7A).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Sato taken with Kunori et al. in view of Tomisawa the feature as taught by Lee in order to facilitate maintaining a uniform voltage across the source line.

Allowable Subject Matter

8. Claims 6 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 6 and 12, the major difference between the teachings of the prior art to record (Pub. No. US 2002/0140643, Sato and USP 6,144,584, Kunori et al.) and that of the instant invention is that said prior art of record **does not teach** a structure wherein the conductive layer comprises at least a conductor located over the branch lines.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,380,636	Tatsukawa et al
Pub. No.	US 2004/00117162	Sato et al..

To Respond

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669.

The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent E. Kovalick
June 1, 2006

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